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10/783,523	02/20/2004	Kuo Sheng Lee	E0523-00072	7163

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EXAMINER	
LIE, ANGELA M	
ART UNIT	**PAPER NUMBER**
2821	

DATE MAILED: 06/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/783,523	LEE, KUO SHENG	
	Examiner	Art Unit	
	Angela M. Lie	2821	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9,10,12-16 and 18-20* is/are rejected.

7)☒ Claim(s) *8,11 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a) because they fail to show element 309 (interconnections) in figure 3; figures 4a and 4b; elements 520, 522, 524, 526, 528, 530, and 532 in figure 5b as described in the specification, and element 514 in figures 5a and 5b is not defined. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 2-3, 14 and 16 are objected to because of the following informalities: Power can not be categorized as positive or negative, therefore phrases such as "positive power" and "negative power" are incorrect. In order to examine objected claims, an examiner considers a "positive power" to be a positive voltage and similarly a "negative power" to be a negative voltage. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-7, 9-10, 12-16 and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Wakimoto et al (US 6690028).

As to claim 1, Wakimoto et al disclose a display comprising: a display area on a substrate (as shown in figure 1, the bottom part of element 1, is a display area since light rays are reflected in downward direction), at least bus line of a first type (column 1, lines 32-33, since a negative voltage is applied to the cathode electrode, it is an inherent fact that there has to be a power bus enabling connection to the power supply),

at least one power bus line of a second type (column 1 lines 31-32, since positive voltage is applied to the anode electrode, inherently there has to be a power bus enabling the flow of current), a cathode layer (Figure 7 element 203) coupled to display elements in the display area (as shown in figure 7 elements 203 and 1) and the power bus line of the first type (column 1 lines 32-33), an insulating layer formed on the cathode (Figure 7 element insulative material), and a power supply plane formed on the insulating layer connected to the power bus line of the first type (column 1 lines 31-32, since anode is connected to the positive voltage (second type), and anode is also in contact with the electrode 81 (power supply plane), therefore power supply plane is connected to the power bus line of the second type), wherein the insulating layer separates the power supply plane from the cathode (as shown in figure 7, an insulating layer creates a separation between a left side of the cathode and the side of element 81 (part pointing downwards), and wherein the power supply provide even distribution of power to the EL elements (since each cathode and anode is supplied with certain voltage (i.e. negative or positive), it is also understood that power distribution is even).

As to claim 2, Wakimoto et al disclose the device wherein the power bus line of the first type is a negative power supply (column 1 lines 32-33).

As to claim 3, Wakimoto et al disclose the device wherein the power bus line of the second type is a positive power supply (column 1 lines 31-32).

As to claim 4, Wakimoto et al disclose the device further comprising one or more power supply lines coupled to the power supply plane (Figure 7 element 81) for providing power to the display elements (column 1 lines 31-33, since cathode and

anode are connected to negative and positive voltage respectively, and those two types of electrodes are also connected to the power supply plane (Figure 7 element 81), inherently power supply lines are coupled to the power supply plane).

As to claim 5, Wakimoto et al disclose the device wherein one or more interconnections are made at different sides of the display area for connecting the power supply plane to the power supply lines (column 1 lines 31-33 and figure 7, since cathode (203) is connected to negative voltage (i.e. first power line) and anode (2) is connected to positive voltage (i.e. second power line), and power plane (81) spreads over right side of substrate (1) and makes connection with cathode (203), and it also spreads over the left side of substrate (1) and makes a connection with anode (2), therefore power supply plane connects with power supply lines on different sides of the display).

As to claim 6, Wakimoto et al disclose the device wherein the interconnections are made at opposite sides of the display area (as shown in figure 7, connection with cathode (203) is on the right side and connection with anode (2) is on the left side).

As to claim 7, Wakimoto et al disclose the device wherein the interconnections are made at adjacent sides of the display area (as shown in figure 7, connection with cathode (203) on the right side is adjacent to the left side where anode (2) has its connection).

As to claims 9 and 15, Wakimoto et al disclose an organic light emission display comprising: a cathode layer (Figure 7 element 203), an insulating layer covering at least one portion of the cathode layer (Figure 7, element insulative material), and a power

supply plane (Figure 7 element 81, since element 81 is an electrode, it is capable of conducting electricity and cathode is connected to a negative voltage (column 1 lines 31-33), therefore the electrode 81 is part of power supply) formed on the insulating layer overlapping the covered portion of the cathode layer to form a predetermined area under which a display area is formed (Figure 7 element 1), wherein the power supply plane provides even distribution of power to the display area (since this structure allow for plural power connections, the distribution of power is inherently uniform). Method for forming power supply for light emission display device as presented in claim 15, is inherent in order to make an apparatus as described in claim 9.

As to claim 10, Wakimoto et al disclose the device wherein the power supply plane (Figure 7 element 81) connects to one or more power supply lines through one or more interconnections (in order to provide a voltage to the cathode it is inherent that that power plane has to be connected (at via cathode or anode) to at least one power supply line).

As to claim 14, Wakimoto et al disclose the device comprising a negative power supply coupled to cathode layer (column 1 lines 32-33).

As to claim 16, Wakimoto et al disclose the method further comprising forming one or more interconnections (forming connection as shown in figure 7, connection between elements 81 and 2) for connecting the power supply plane (81) to one or more power supply lines (column 1, lines 31-32, since anode (2) is connected to positive voltage, and it is also connected to power plane (81), therefore power plane is

connected to positive voltage via anode) that provide positive voltage to one or more display element (2) in the display area (1).

As to claims 12 and 18, Wakimoto et al disclose the device wherein the power supply lines are in a mesh form (column 1 lines 49-53, since anode lines (Figure 6 element 21) and cathode lines (Figure 6 element 71) are orthogonal to each other (mesh or matrix form), and there is a different voltage supplied to those electrodes (column 1 lines 31-33), therefore it is inherent that power lines will have mesh form as well).

As to claims 13 and 19, Wakimoto et al disclose the device and therefore a method, wherein the interconnections are formed in areas of the power supply plane that do not overlap with the insulating layer (as shown in figure 7, anode (2) is connected to power supply plane (81) in the place where it does not overlap with the insulating layer (insulative layer)).

As to claim 20, Wakimoto et al disclose the method further comprising forming one or more interconnections for connecting the cathode layer to at least one power bus line in an area that do not overlap with the insulating layer (column 1 lines 32-33, Wakimoto et al disclose that there is a connection allowing for negative voltage to be supplied to the cathode, inherently in the place of connection between the voltage source and cathode, there is no isolation layer because otherwise connection could not be made, and voltage could not be supplied).

5. Claims 8, 11 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Allowable Subject Matter

6. The following is a statement of reasons for the indication of allowable subject matter:

As to claim 8, the prior art failed to teach the device wherein the power supply plane connects to an anode of each display element though a via connection.

As to claim 11, the prior art fail to teach the device wherein the interconnections are made at two ends of the power supply lines.

As to claim 17, the prior art fail to teach the method wherein the interconnections are formed at two ends of each power supply line (interconnection is specified in claim 16).

The Prior Art

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- US 6307324 discloses a display apparatus using electroluminescence elements
- US 6828723 discloses an EL display device

- US 20030063081 discloses a pixel circuit, display apparatus and electronic apparatus equipped with current driving type light-emitting device
- US 20030111954 discloses a flat panel display device with face plate and method for fabricating the same
- US 20040080470 discloses a light emitting device with less uneven brightness.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angela M. Lie whose telephone number is 571-272-8445. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don Wong can be reached on 571-272-1834. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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